

### Remarks

In view of the following amendments and remarks, favorable reconsideration of the outstanding office action is respectfully requested. Claims 1 – 34 remain in this application. Claims 1 – 30, 30b, and 31 - 33 have been renumbered as claims 1 – 34.

#### **1. Examiner Interview**

Applicants' representative wishes to express his appreciation to Examiner Jackson for the courtesy extended to him during the interview conducted on or about February 15, 2005.

#### **2. Allowable Subject Matter**

Applicants note with appreciation that the Examiner has indicated the subject matter of claim 24 is are patentable, and would be allowable if rewritten in independent form.

#### **3. Claim Numbering**

The Examiner rightly pointed out in his Rejection under 35 U.S.C. §103(a) that the claims were not properly numbered under 37 C.F.R. §1.75(f) in that they contained a claim 30b. The applicants have renumbered the claims and have provided a new set of properly numbered original claims. Claims 1- 30 maintain their original numbering. Claim 30b is renumbered as claim 31. Claims 31 – 33 now become claims 32 – 34. Accordingly, claims 1 – 34 are currently pending.

#### **4. Priority**

##### A. Request for Correction of Inventorship in Response to Claim of Priority from Co-pending U.S. Application Serial No. 09/827,007

This is a request to correct the inventorship under 37 C.F.R. §1.48(a). M.P.E.P. §201.03 states that correction of inventorship in an application is permitted by amendment under 35 U.S.C. §116 which is implemented by 37 C.F.R. §1.48. 37 C.F.R. §1.48(a) is directed at correcting the inventorship in an application where the inventorship was improperly set forth in the executed oath or declaration filed in the application. In this case, the original declaration claimed priority to U.S. Application Serial No. 09/827,007, now U.S. Patent No. 6,621,388 (Macbeth), under 35 U.S.C. §120. However, the inventorship was

improperly set forth in the executed declaration filed in the application because the name of Bruce F. Macbeth was omitted from said executed declaration. Accordingly, please correct the inventorship of the present invention under 37 C.F.R. §1.48(a) to add Bruce F. Macbeth. The inventorship as properly set forth should include Thomas Packard, Dejan Radosavljevic, and Bruce F. Macbeth.

In addition to “a request to correct the inventorship that sets forth the desired inventorship change,” an amendment of the inventorship under 37 C.F.R. §1.48(a) must satisfy four (4) additional requirements.

(1) 37 C.F.R. §1.48(a) requires *a statement from each person being added as an inventor and from each person being deleted as an inventor that the error in inventorship occurred without deceptive intention on his or her part*. A statement from the inventor being added, Bruce F. Macbeth, is attached hereto.

(2) 37 C.F.R. §1.48(a) requires *an oath or declaration by the actual inventor or inventors as required by § 1.63*. A declaration and assignment which properly sets forth the inventorship is also attached hereto as required by 37 C.F.R. § 1.63.

(3) 37 C.F.R. §1.48(a) requires *the written consent of the assignee under 37 C.F.R. §3.73(b) if an assignment has been executed by any of the original named inventors*. Since an assignment was executed by the original named inventors, agreeing to correction of inventorship in accordance with 37 C.F.R. §3.73(b) is also attached hereto.

(4) Finally, 37 C.F.R. §1.48(a) requires *the processing fee set forth in § 1.17(i)*. The processing fee as set forth in 37 C.F.R. § 1.17(i) is also attached hereto.

According to M.P.E.P §1002.02 (d), a request for correction of inventorship under 37 C.F.R. §1.48(a) is decided by a Supervisory Patent Examiner. Because all of the requirements under 37 C.F.R. §1.48(a) to correct the inventorship have been satisfied, the applicants respectfully request that the inventorship be changed.

Applicants also respectfully request that the claim of priority from co-pending U.S. Application Serial No. 09/827,007, filed April 5, 2001, be granted. The condition regarding common inventorship is satisfied under 35 U.S.C. §120 in light of the correction of inventorship.

B. Claim of Priority to U.S. Provisional Patent Application Serial No. 60/326,531  
Under 35 U.S.C. 119(e)

The applicants respectfully request that the applicants claim of priority from U.S. Provisional Application Serial No. 60/326,531 also be granted in light of the correction of inventorship. As noted above, the condition regarding common inventorship is satisfied under 35 U.S.C. §120.

**5. § 102 Rejections**

The Examiner has rejected claims 1 – 23 and 25 - 33 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,621,388 to Macbeth. The applicants traverse the rejection because Macbeth is not prior art under 35 U.S.C. § 102.

Claims 1- 23, 25 – 30, and 31 – 33, which have been renumbered as claims 1- 23, 25 – 30, and 32 – 34, are allowable under 35 U.S.C. § 102(e). Accordingly, the applicants respectfully request that the rejection under 35 U.S.C. § 102(e) be withdrawn.

**6. § 103 Rejections**

The Examiner has rejected claim 30b under 35 U.S.C. § 103(a) as being unpatentable for obviousness over Macbeth in view of U.S. Patent No. 6,309,248 to King. The applicants traverse the rejection because Macbeth is not prior art under 35 U.S.C. § 102, and therefore is not prior art under 35 U.S.C. § 103(a).

Claim 30b, which has been renumbered as claim 31, is allowable under 35 U.S.C. § 103(a). Accordingly, the applicants respectfully request that the rejection under 35 U.S.C. § 103(a) be withdrawn.

## 7. Conclusion

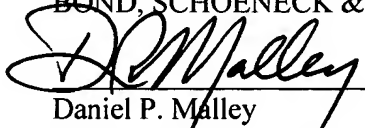
Based upon the amendments, remarks, and papers of record, Applicant believes the pending claims of the above-captioned application are in allowable form and patentable over the prior art of record. Applicant respectfully requests reconsideration of the pending claims 1 – 34 and a prompt Notice of Allowance thereon.

Applicant believes that a two-month extension of time is necessary to make this Response timely. The appropriate fee is attached hereto. Should Applicant be in error, Applicant respectfully requests that the Office grant such time extension pursuant to 37 C.F.R. § 1.136(a) as necessary to make this Response timely, and hereby authorizes the Office to charge any necessary fee or surcharge with respect to said time extension to the deposit account of the undersigned firm of attorneys, Deposit Account 50-1546.

Please direct any questions or comments to Daniel P. Malley at (607) 330-4010.

Respectfully submitted,

Date: 4/19/05

BOND, SCHOENECK & KING, PLLC  
  
Daniel P. Malley  
Registration No. 43,443  
BOND, SCHOENECK & KING, PLLC  
10 Brown Rd.  
Suite 201  
Ithaca, NY  
14850-1248

**Renumbered Claims**

This listing of claims will replace all prior versions and listings of claims in the application.

**Listing of claims:**

1. (original) A protective device including a plurality of line terminals configured to be connected to an electrical distribution system and a plurality of load terminals configured to be connected to at least one load, comprising:
  - a fault detection circuit coupled to the plurality of line terminals and the plurality of load terminals, the fault detection circuit being configured to detect at least one fault condition;
  - a power interruption circuit coupled to the fault detection circuit, the power interruption circuit including a set of movable contacts configured to decouple the plurality of line terminals from the plurality of load terminals in response to the fault detection circuit detecting the at least one fault condition;
  - a reset mechanism coupled to the power interruption circuit and configured to actuate the movable contacts to re-couple the plurality of line terminals to the plurality of load terminals;
  - a lock-out mechanism coupled to the reset mechanism, the lockout mechanism being configured to disable the reset mechanism in a lock-out state; and
  - a test circuit coupled to the fault detection circuit and the lock-out mechanism, the test circuit being configured to provide a simulated fault signal to the fault detection circuit in response to a user stimulus, the test circuit being configured to drive the lock-out mechanism from an unlocked state to the lock-out state if the fault detection circuit and/or power interruption circuit fails to respond to the simulated fault signal within a predetermined period of time.
2. (original) The device of claim 1, wherein the fault detection circuit includes a ground fault detection circuit.

3. (original) The device of claim 1, wherein the fault detection circuit includes an arc fault detection circuit.

4. (original) The device of claim 1, wherein the reset mechanism further comprises:

a reset button; and

a linkage mechanism coupled to the reset button, the linkage mechanism being configured to engage a portion of the movable contacts in a coupled state, the set of movable contacts being engaged to thereby couple the plurality of line terminals to the plurality of load terminals, the linkage mechanism also being configured to disengage the portion of the movable contacts in a decoupled state, such that the plurality of line terminals are decoupled from the plurality of load terminals.

5. (original) The device of claim 4, wherein the reset mechanism further comprises a latch coupled to the linkage mechanism, the latch being configured to move the linkage mechanism from the coupled state to the decoupled state in response to a stimulus from the power interruption circuit.

6. (original) The device of claim 5, wherein the latch is configured to move the linkage from the uncoupled state to the coupled state in response to a user stimulus of the reset button, when the test circuit is in the unlocked state.

7. (original) The device of claim 5, wherein the latch cannot move the linkage from the uncoupled state to the coupled state in response to a user stimulus of the reset button, when the test circuit is in the lock-out state.

8. (original) The device of claim 5, wherein the latch is coupled to a fuse mechanism, the fuse mechanism being closed in the unlocked state and open in the lock-out state, the fuse mechanism being configured to prevent the latch from latching the linkage mechanism when the test circuit is in the lock-out state.

9. (original) The device of claim 5, wherein the lockout mechanism further comprises:  
a spring mechanism configured to move the latch into the lock-out state; and  
a fuse mechanism coupled to the spring mechanism, the fuse mechanism being  
configured to prevent the spring mechanism from moving the latch into the  
lock-out state, the use mechanism being configured to fail if the fault detection  
circuit and/or power interruption circuit fails to respond to the simulated fault  
signal within the predetermined period of time.

10. (original) The device of claim 9, wherein the fuse mechanism includes a resistor soldered  
in a position corresponding to the unlocked state, the test circuit being configured to transmit  
current through the resistor when providing the simulated fault signal, the current being  
configured to cause the solder to fail after the predetermined period of time elapses, to  
thereby allow the spring mechanism to move the latch into the lock-out state.

11. (original) The device of claim 9, wherein the fuse mechanism includes a resistor disposed  
in a position corresponding to the unlocked state by an adhesive, the test circuit being  
configured to transmit current through the resistor when providing the simulated fault signal,  
the current being configured to cause the adhesive to fail after the predetermined period of  
time elapses, to thereby allow the spring mechanism to move the latch into the lock-out state.

12. (original) The device of claim 1, wherein the lock-out mechanism further comprises:  
a spring mechanism configured to drive the reset mechanism into the lock-out state;  
and  
a fuse mechanism coupled to the spring mechanism, the fuse mechanism being  
configured to prevent the spring mechanism from driving the lockout  
mechanism into the lock-out state, the fuse mechanism being configured to fail  
if the fault detection circuit and/or power interruption circuit fails to respond to  
the simulated fault signal within the predetermined period of time.

13. (original) The device of claim 12, wherein the fuse mechanism includes a resistor  
soldered in a position corresponding to the unlocked state, the test circuit being configured to  
transmit an electric current through the resistor when providing the simulated fault signal, the

electric current being configured to cause the solder to fail after the predetermined period of time elapses, to thereby allow the spring mechanism to move the lockout mechanism into the lock-out state.

14. (original) The device of claim 12, wherein the fuse mechanism includes a resistor disposed in a position corresponding to the unlocked state by an adhesive, the test circuit being configured to transmit current through the resistor when providing the simulated fault signal, the current being configured to cause the adhesive to fail after the predetermined period of time elapses, to thereby allow the spring mechanism to move the lockout mechanism into the lock-out state.

15. (original) The device of claim 1, wherein the lock-out mechanism includes a resistor coupled to the reset mechanism by a material, the material being configured to fail when the predetermined period of time elapses to decouple the resistor from the reset mechanism, the reset mechanism being driven into the lock-out state.

16. (original) The device of claim 15, wherein the material includes solder.

17. (original) The device of claim 15, wherein the material includes an adhesive.

18. (original) The device of claim 1, wherein the test circuit further comprises:

- a test switch responsive to a user stimulus;

- a first circuit element coupled to the test button, the first circuit element configured to generate the at least one fault condition in response to the test switch being in a closed position; and a second circuit element coupled to the test switch, the second circuit element being configured to drive the test circuit from the unlocked state to the lock-out state if the fault detection circuit and/or the power interruption circuit fail to respond to the at least one fault condition within the predetermined time period.

19. (original) The device of claim 18, wherein the second circuit element includes a fuse mechanism that is closed in the unlocked state and open in the lock-out state.



20. (original) The device of claim 18, wherein the second circuit element includes a resistor coupled to the lockout mechanism by solder, the solder being configured to fail after the predetermined time elapses, decoupling the resistor from the lock-out mechanism, driving the test circuit from the unlocked state to the lock-out state.

21. (original) The device of claim 18, wherein the first circuit element produces a differential current when the test switch is closed, the differential current simulating the at least one fault condition, the second circuit element generating substantially no differential current.

22. (original) The device of claim 18, wherein the second circuit element includes a resistor coupled to the reset mechanism by a material, the material being configured to fail when the predetermined period of time elapses to decouple the resistor from the reset mechanism, the reset mechanism being driven into the lock-out state.

23. (original) The device of claim 22, wherein the lock-out mechanism further comprises:  
a spring mechanism configured to drive the reset mechanism into the lock-out state;  
and  
the resistor coupled to the spring mechanism, the resistor being configured to prevent the spring mechanism from driving the lockout mechanism into the lock-out state, the resistor being configured to fail if the fault detection circuit and/or power interruption circuit fails to respond to the simulated fault signal within the predetermined period of time.

24. (original) The device of claim 18, wherein the second circuit element further comprises:  
a first resistor coupled to the test switch;  
a transistor including a base, emitter, and collector terminals, the base terminal being coupled to the first resistor; and  
a second resistor coupled to the collector terminal and soldered to the lockout mechanism, the solder being configured to fail after the predetermined time elapses, decoupling the second resistor from the lock-out mechanism, driving the test circuit from the unlocked state to the lock-out state.

25. (original) The device of claim 1, wherein the power interruption circuit includes a spring loaded mechanism configured to actuate the set of movable contacts from a coupled state to an uncoupled state.

26. (original) The device of claim 25, wherein the reset mechanism drives the set of movable contacts from the uncoupled state to the coupled state in the unlocked state, but cannot drive the set of movable contacts from the uncoupled state to the coupled state in the lock-out state.

27. (original) The device of claim 1, wherein the power interruption circuit includes a relay mechanism configured to actuate the set of movable contacts from a coupled state to an uncoupled state.

28. (original) The device of claim 27, wherein the reset mechanism drives the set of movable contacts from the uncoupled state to the coupled state in the unlocked state, but cannot drive the set of movable contacts from the uncoupled state to the coupled state in the lock-out state.

29. (original) The device of claim 1, wherein the power interruption circuit includes a bus bar mechanism configured to actuate the set of movable contacts from a coupled state to an uncoupled state.

30. (original) The device of claim 29, wherein the reset mechanism drives the set of movable contacts from the uncoupled state to the coupled state in the unlocked state, but cannot drive the set of movable contacts from the uncoupled state to the coupled state in the lock-out state.

[[30b.]] 31. (amended) The device of claim 1, wherein the device further comprises one of a receptacle, switch, circuit breaker, module, and portable housing containing the device.

[[31]] 32. (amended) A protective device including a plurality of line terminals configured to be connected to an electrical distribution system and a plurality of load terminals configured to be connected to at least one load, comprising:

- a fault detection circuit coupled to the plurality of line terminals and the plurality of load terminals, the fault detection circuit being configured to detect at least one fault condition;
- a power interruption circuit coupled to the fault detection circuit, the power interruption circuit including a set of movable contacts configured to decouple the plurality of line terminals from the plurality of load terminals in response to the fault detection circuit detecting the at least one fault condition;
- a reset mechanism coupled to the power interruption circuit and configured to actuate the movable contacts to re-couple the plurality of line terminals to the plurality of load terminals;
- a lock-out mechanism coupled to the reset mechanism, the lockout mechanism including a spring mechanism configured to drive the reset mechanism into a lock-out state, and a fuse element coupled to the spring mechanism to prevent the spring mechanism from moving in an unlocked state; and
- a test circuit coupled to the fault detection circuit and the lock-out mechanism, the test circuit being configured to provide a simulated fault signal to the fault detection circuit, the test circuit being configured to open the fuse element to thereby drive the lock-out mechanism from the unlocked state to the lock-out state if the fault detection circuit and/or power interruption circuit fails to respond to the simulated fault signal within a predetermined period of time.

[[32]] 33. (amended) The device of claim 32, wherein the fuse mechanism includes a resistor.

[[33]] 34. (amended) A protective device including a plurality of line terminals configured to be connected to an electrical distribution system and a plurality of load terminals configured to be connected to at least one load, comprising:

- a fault detection circuit coupled to the plurality of line terminals and the plurality of load terminals, the fault detection circuit being configured to detect at least one fault condition;
- a power interruption circuit coupled to the fault detection circuit, the power interruption circuit including a set of movable contacts configured to decouple

the plurality of line terminals from the plurality of load terminals in response to the fault detection circuit detecting the at least one fault condition;

a reset mechanism coupled to the power interruption circuit and configured to actuate the movable contacts to re-couple the plurality of line terminals to the plurality of load terminals;

a lock-out mechanism coupled to the reset mechanism, the lockout mechanism being configured to disable the reset mechanism in a lock-out state; and

a test circuit including a first circuit element coupled to the fault detection circuit and a second circuit element coupled to the lock-out mechanism, the first circuit element being configured to provide a simulated fault signal to the fault detection circuit, the second circuit element being configured to drive the lock-out mechanism from an unlocked state to the lock-out state if the fault detection circuit and/or power interruption circuit fails to respond to the simulated fault signal within a predetermined period of time.